Abstract of the Disclosure

A method of fabricating a sub-micron MOS transistor includes preparing a substrate, including isolating an active region therein; depositing a gate oxide layer; depositing a first selective etchable layer over the gate oxide layer; depositing a second selective etchable layer over the first selective etchable layer; etching the structure to undercut the first selective etchable layer; implanting ions in the active region to form a source region and a drain region; depositing and planarizing the oxide; removing the remaining first selective etchable layer and the second selective etchable layer; depositing a gate electrode; and depositing oxide and metallizing the structure. A sub-micron MOS transistor includes a substrate; and an active region, including a gate region having a length of less than one micron; a source region including a LDD source region; and a drain region including a LDD drain region.